

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



10/525987



(43) International Publication Date
18 March 2004 (18.03.2004)

PCT

(10) International Publication Number
WO 2004/023536 A1

(51) International Patent Classification⁷: H01L 21/20

(74) Agents: HARDING, Richard, Patrick et al.; Marks & Clerk, 4220 Nash Court, Oxford Business Park South, Oxford, Oxfordshire OX4 2RU (GB).

(21) International Application Number:
PCT/GB2003/003514

(22) International Filing Date: 12 August 2003 (12.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0220438.6 3 September 2002 (03.09.2002) GB

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(71) Applicant (*for all designated States except US*): UNIVERSITY OF WARWICK [GB/GB]; Coventry, Warwickshire CV4 7AL (GB).

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(72) Inventors; and

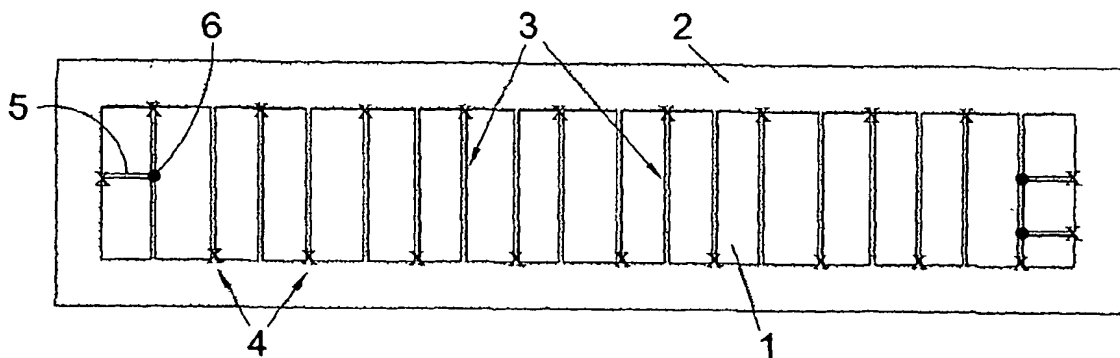
(75) Inventors/Applicants (*for US only*): CAPEWELL, Adam, Daniel [GB/GB]; 16 Cowdray Close, Leamington Spa, Warwickshire CV31 1LB (GB). GRASBY, Timothy, John [GB/GB]; 3 Clover Cottage, Station Road, Salford Priors, Worcestershire WR11 8UX (GB). PARKER, Evan, Horatio, Charles [GB/GB]; The Orchard, Back Ends, Chipping Campden, Gloucestershire GL55 6AU (GB). WHALL, Terence [GB/GB]; 10 Purshall Close, Redditch, Worcestershire B97 4PD (GB).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FORMATION OF LATTICE-TUNING SEMICONDUCTOR SUBSTRATES



(57) Abstract: A method of forming a lattice-tuning semiconductor substrate comprises the steps of defining parallel strips of a Si surface by the provision of spaced parallel oxide walls (2) on the surface, selectively growing a first SiGe layer on the strips such that first dislocations (3) extend preferentially across the first SiGe layer between the walls (2) to relieve the strain in the first SiGe layer in directions transverse to the walls (2), and growing a second SiGe layer on top of the first SiGe layer to overgrow the walls (2) such that second dislocations form preferentially within the second SiGe layer above the walls (2) to relieve the strain in the second SiGe layer in directions transverse to the first dislocations (3). The dislocations so produced serve to relax the material in two mutually transverse directions whilst being spatially separated so that the two sets of dislocations cannot interact with one another. Thus the density of threading dislocations and the surface roughness is greatly reduced, thus enhancing the performance of the virtual substrate by decreasing the disruption of the atomic lattice that can lead to scattering of electrons in the active devices and degradation of the speed of movement of the electrons.

WO 2004/023536 A1